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Date: August 18, 2005

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/986,262

Filing Date: 11/08/2001

Applicant: Gudmunson et al.

Title: METHOD AND APPARATUS FOR THE DATA-DRIVEN SYNCHRONOUS PARALLEL PROCESSING OF DIGITAL DATA

AMENDMENT

In response to the Official Action
Dated: 04/20/2005

Examiner: Tonia L. Meonske

Attorney's Ref.: 663-169/MBE

Commissioner for Patents
U.S. Patent and Trademark Office
220 20th Street South
Customer Window, **Mail Stop Amendment**
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Arlington, VA 22202
U.S.A.

Dear Sir:

IN THE CLAIMS

1. (Original) A method for data-driven synchronous parallel processing of a stream of data packets by multiple data processing units working in parallel, comprising the steps of:

a. distributing at least one instruction for data processing to one data processing unit of the

multiple data processing units, before the data processing unit is available to process the instruction;

b. storing the instruction in an execution instructions memory;

c. sending from the one data processing unit a data request for at least one data packet corresponding to the instruction, required to execute the instruction;

d. storing a record of the at least one data packet requested;

e. associating with the at least one data packet an address of the one data processing unit;

f. associating with the each data packet sent out a data token showing the readiness of the packet for further processing;

g. when the at least one data packet is received by the processing unit, associating the data packet with the corresponding instruction and distributing the data packet to the one data processing unit; and

h. processing the data according to the corresponding instruction.

2. (Original) The method of claim 1 wherein instructions are distributed to the multiple data processing units consecutively.

3. (Original) The method of claim 1 wherein instructions are distributed to the multiple data processing units concurrently.

4. (Original) The method of claim 1 including, after step f., the step of putting the requested data packets into an internal data buffer in a data processing unit.

5. (Original) The method of claim 1 including, after step g., the step of erasing the record of the data request corresponding to the data packet.

6. (Original) The method of claim 1 including, during step g., the step of sending to the corresponding instruction in the execution instructions memory an indication that the at least one data packet has been received by the processing unit and is available for processing.

7. (Original) The method of claim 1 including, during step c., the step of associating with the data packets an address of its sender and, during the step g, associating the data packet with the corresponding instruction according to the address of the data packet sender.

8. (Original) The method of claim 1 including, during the step g, associating the data packet with the corresponding instruction according to the order of the data packet received.

9. (Original) The method of claim 4 including the step of retrieving each data packet from the internal data buffer to be processed according to the corresponding instruction.

10. (Original) The method of claim 1 wherein an output of the processing step is sent to another data processing unit or out of the processor, or both.

11. (Original) The method of claim 1 wherein processing occurs in real-time.

12. (Withdrawn) A method of providing a substantially non-stalling sequential flow of data packets through a digital data-driven processor, the digital processor storing at least one instruction for processing data packets in accordance with the instruction, comprising the steps of:

a. providing a buffer between adjacent units processing, distributing or otherwise handling the data;

b. providing a fullness signal indicating a fullness state of the buffer from the data buffer to a previous adjacent unit, before the buffer is full;

c. providing an emptiness signal indicating an emptiness state of the buffer from the data buffer to a next adjacent unit, before the buffer is empty;

d. providing an incoming data validity signal for synchronization of data handling by the buffer with the arrival of a data packet to the buffer; and

e. providing an outgoing data validity signal for synchronization of data handling by a unit next after the buffer with an outgoing data packet from the buffer,

wherein assertion of the fullness signal in advance of filling the buffer allows the buffer to absorb data packets in transit between a previous unit sending the data and the buffer receiving the data, and assertion of the emptiness signal in advance of depleting the buffer allows for the processor to request new data packets before the buffer becomes empty.

13. (Withdrawn) The method of claim 12 wherein the validity signal comprises a data token.

14. (Withdrawn) The method of claim 13 in a processor having a plurality of processing units, including the step of programming a timing of assertion of the fullness signal and of the emptiness signal to allow for management of synchronous data flow to the processing units.

15. (Withdrawn) An apparatus for substantially non-stalling synchronous data packet flow through a digital data-driven processor, each data packet being associated with an address of a processing unit containing an instruction for processing the data packet, comprising a data buffer for temporary storage of the data packets, the buffer comprising

an input port for receiving incoming data packets and their associated addresses;

an output port for sending out outgoing data and their associated addresses;

an input port for receiving an incoming validity signal;

an output port for sending an outgoing validity signal;

an outgoing fullness signal indicating a fullness of the buffer, adapted to be asserted in advance of the filling of the buffer;

an outgoing emptiness signal indicating an emptiness of the buffer, adapted to be asserted in advance of the depletion of the buffer; and

control logic for regulating a timing of assertion of the fullness and the emptiness signals in a multi-processing system.

16. (Withdrawn) The apparatus of claim 15 wherein the validity signal comprises a data token.

17. (Withdrawn) The apparatus of claim 16 wherein the buffer comprises a FIFO buffer.

18. (Amended) An apparatus for substantially non-stalling data-driven synchronous parallel processing of data packets including a digital data processor, further comprising:

an interface for receiving instructions and digital data from at least one external device and sending instructions or digital data or both to at least one external device;

an instruction path contained inside the processor;

a data path, separate from the instruction path, contained inside the processor;

a plurality of data processing units organized for parallel processing of the data; and

a distributing unit organized for distributing one or more instructions at a time to the data processing units.

19. (Original) The apparatus of claim 18 wherein instructions are distributed to the plurality of data processing units consecutively.

20. (Original) The apparatus of claim 18 wherein instructions are distributed to the plurality of data processing units concurrently.

21. (Original) The apparatus of claim 18 wherein each data processing unit comprises

a storage for instructions;

a storage for records of outstanding data requests;

a storage for receiving requested data packets; and

a computation module for processing the requested data packets in accordance with at least one associated instruction.

22. (Original) The apparatus of claim 21 comprising control logic for controlling instruction and data flows through the processor.

23. (Original) The apparatus of claim 18 wherein the digital data processor comprises a general-purpose microprocessor.

24. (Original) The apparatus of claim 18 wherein the digital data processor comprises a graphics processor.

25. (Original) The apparatus of claim 18 wherein the digital data processor comprises a digital signal processor.

26. (Original) The apparatus of claim 21 wherein the computational module operates using vector values.

27. (Original) The apparatus of claim 21 wherein the computational module operates using scalar values.

28. (Original) A method for data-driven synchronous parallel processing of a stream of data packets by multiple data processing units working in parallel, comprising the steps of:

a. distributing at least one instruction for data processing to one data processing unit of the multiple data processing units, before the data processing unit is available to process the instruction;

b. storing the instruction in an execution instructions memory;

c. sending from the one data processing unit a data request for at least one data packet corresponding to the instruction, required to execute the instruction;

d. storing a record of the at least one data packet requested;

e. associating with the at least one data packet an address of the one data processing unit;

f. associating with the at least one data packet a data token indicating a readiness of the data packet for further processing and comprising data for associating the at least one data packet with the corresponding instruction at the one data processing unit;

g. when the at least one data packet is received by the processing unit, associating the data packet with the corresponding instruction and distributing the data packet to the one data processing unit; and

h. processing the data according to the corresponding instruction.